Exhibit A – Part 2

EXHIBIT 4

Brad Kohn
<BKohn@memc.com>

11/18/2005 12:33 PM

To: "Jacques-Elie LEVY" <jacques-elie.levy@soitec.fr>
cc: "Emmanuel HUYGHE" <emmanuel.huyghe@soitec.fr>, GNeuner@eapdlaw.com, "Brody, Michael" <MBrody@winston.com>
Subject: Re: TR: MEETING WITH SOITEC

Mr. Levy,
Thanks for your email note dated November 11, 2005. While we were initially encouraged by Soitec's November 8 proposal to meet with us to have a discussion about our allegations of Soitec infringement, I am sorry to say that we were disappointed with the Soitec list of proposed attendees for the proposed December 2, 2005 meeting. We were disappointed with the list because we believe the list is likely too short in that it does not appear to include senior executives with decision-making authority.

Let me be clear about what we believe the purpose of this meeting must be, in order to make the meeting worthwhile for MEMC: we expect Soitec to arrive with a specific proposal that addresses how Soitec intends to remedy what we believe is significant past infringement and continuing infringement. Based on your list of proposed attendees, we do not believe that Soitec's purpose for the meeting is to present MEMC with a legitimate, thoughtful substantive proposal to address what we believe is significant past and current infringement. If Soitec's purpose for the meeting is instead to show up in St. Peters and explain to us why Soitec is not infringing our intellectual property, then I would respectfully submit to you that the meeting will not be worth it from our perspective, and you should not waste your time flying to St. Louis for such a meeting. Instead, please just send us that information in writing by November 22, 2005 so that we may evaluate your position.

Candidly, and forgive me for the blunt statement, right now it appears to us that the proposed December 2 meeting is yet another stalling tactic by Soitec. The time for stalling is over. Soitec has been on notice of our allegations of infringement for over a year. Another meeting to debate that point with us is worthless to MEMC. There are more appropriate forums in which to have that debate. We believe that a meeting between MEMC and Soitec, should it occur, should be held to avoid such a forum, not just to delay or preview such a forum.

Again, we remain happy to meet with Soitec to receive a specific proposal that addresses how Soitec intends to remedy what we believe is significant past and current infringement. If that is not Soitec's intended purpose and agenda for the meeting, then there is no need to convene such a meeting. I look forward to hearing from you about this. If your response indicates that a meeting will be fruitful, I will work with people's schedules here to make it happen.

Regards,
Brad Kohn

Bradley D. Kohn
Vice President and General Counsel
MEMC Electronic Materials, Inc.
636-474-7313 telephone
636-474-5180 fax
bkohn@memc.com

==========

==========

EXHIBIT 5

US006236104B1

(12) **United States Patent**
Falster

(10) **Patent No.: US 6,236,104 B1**
(45) **Date of Patent: *May 22, 2001**

(54) **SILICON ON INSULATOR STRUCTURE FROM LOW DEFECT DENSITY SINGLE CRYSTAL SILICON**

(75) Inventor: **Robert J. Falster**, Milan (IT)

(73) Assignee: **MEMC Electronic Materials, Inc.**, St. Peters, MO (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/387,288**

(22) Filed: **Aug. 31, 1999**

Related U.S. Application Data

(60) Provisional application No. 60/098,902, filed on Sep. 2, 1998.

(51) **Int. Cl.**[7] **H01L 29/06**; H01L 27/01; H01L 27/12; H01L 31/0392

(52) **U.S. Cl.** **257/618**; 257/347; 257/913

(58) **Field of Search** 257/347, 618, 257/913

(56) ***References Cited***

U.S. PATENT DOCUMENTS

4,314,595	2/1982	Yamamoto et al.	148/1.5
4,376,657	3/1983	Nagasawa et al.	148/1.5

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

39 05 626 A1	8/1989	(DE)	C30B/15/20
43 23 964 A1	1/1994	(DE)	H01L/21/324
44 14 947 A1	8/1995	(DE)	C30B/15/20
198 06 045 A1	8/1998	(DE)	C30B/15/20
02180789	7/1990	(EP)	C30B/15/20
04108682	4/1992	(EP)	C30B/15/00
0 503 816 B1	9/1992	(EP)	C30B/33/02
0 504 837 A2	9/1992	(EP)	C30B/15/00
0 536 958 A1	4/1993	(EP)	C30B/15/00
0 716 168 A1	6/1996	(EP)	C30B/15/14
0 799 913 A1	10/1997	(EP)	C30B/15/00
0 962 556 A1	8/1999	(EP)	C30B/15/00
2182 262	5/1987	(GB)	C30B/15/20
3-9078	2/1991	(JP)	C30B/29/06
5-155700	6/1993	(JP)	C30B/33/02
7-201874	8/1995	(JP)	H01L/21/322

(List continued on next page.)

OTHER PUBLICATIONS

Falster, R., et al., "The Engineering of Silicon Wafer Material Properties Through Vacancy Concentration Profile Control and the Achievement of Ideal Oxygen Precipitation Behavior", Mat. Res. Soc. Symp. Proc., vol. 510, pp. 27–35, 1998.

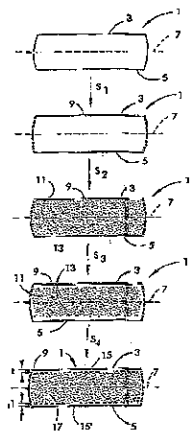
(List continued on next page.)

Primary Examiner—Ngân V. Ngô
(74) *Attorney, Agent, or Firm*—Senniger, Powers, Leavitt & Roedel

(57) **ABSTRACT**

The present invention relates to a silicon on insulator ("SOI") structure having a low defect density device layer and, optionally, a handle wafer having improved gettering capabilities. The device layer comprises a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge, and a first axially symmetric region which is substantially free of agglomerated intrinsic point defects. Additionally, the present invention is directed to such a SOI structure which has a Czochralski single crystal silicon handle wafer which is capable of forming an ideal, non-uniform depth distribution of oxygen precipitates upon being subjected to the heat treatment cycles of essentially any arbitrary electronic device manufacturing process.

40 Claims, 35 Drawing Sheets



U.S. PATENT DOCUMENTS

4,437,922	3/1984	Bischoff et al.	156/603
4,505,759	3/1985	O'Mara	148/1.5
4,548,654	10/1985	Tobin	148/1.5
4,851,358	7/1989	Huber	437/10
4,868,133	9/1989	Huber	437/10
4,981,549	1/1991	Yamashita et al.	156/620.4
5,024,723 *	6/1991	Goesele .	
5,189,500	2/1993	Kusunoki	359/72
5,264,189	11/1993	Yamashita et al.	422/249
5,327,007	7/1994	Imura et al.	257/610
5,401,669	3/1995	Falster et al.	437/12
5,403,406	4/1995	Falster et al.	148/33.2
5,436,175 *	7/1995	Nakato et al.	437/24
5,445,975	8/1995	Gardner et al.	437/10
5,474,020	12/1995	Bell et al.	117/20
5,478,408	12/1995	Mitani et al.	448/33.3
5,485,803	1/1996	Habu	117/14
5,487,354	1/1996	von Ammon et al.	117/13
5,502,010	3/1996	Nadahara et al.	437/247
5,502,331	3/1996	Inoue et al.	257/617
5,534,294	7/1996	Kubota et al.	427/255
5,539,245	7/1996	Imura et al.	257/610
5,593,494	1/1997	Falster	117/2
5,611,855	3/1997	Wijaranakula	117/2
5,659,192	8/1997	Sarma et al.	257/347
5,667,584	9/1997	Takano et al.	117/13
5,674,756	10/1997	Satoh et al.	437/10
5,704,973	1/1998	Sakurada et al.	117/15
5,728,211	3/1998	Takano et al.	117/14
5,738,942	4/1998	Kubota et al.	428/428
5,788,763	8/1998	Hayashi et al.	117/2
5,939,770	8/1999	Kageyama	257/611
5,944,889	8/1999	Park et al.	117/94
5,954,873	9/1999	Hourai et al.	117/13
5,968,262	10/1999	Saishouji et al.	117/13
5,968,264	10/1999	Iida et al.	117/30
5,994,761 *	11/1999	Falster et al.	257/611
6,045,610	4/2000	Park et al.	117/13

FOREIGN PATENT DOCUMENTS

7321120	12/1995	(JP)	H01L/21/322
7335657	12/1995	(JP)	H01L/21/322
8-045945	2/1996	(JP)	H01L/21/322
8045944	2/1996	(JP) .	
8045947	2/1996	(JP)	H01L/21/322
8-268794	10/1996	(JP)	C30B/15/20
8-293589	11/1996	(JP)	H01L/27/12
8-330316	12/1996	(JP)	H01L/21/322
9-199416	7/1997	(JP)	H01L/21/20
9-202690	8/1997	(JP)	C30B/15/22
9-326396	12/1997	(JP)	H01L/21/322
11-067781	3/1999	(JP)	H01L/21/322
11-150119	6/1999	(JP)	H01L/21/322
11-157995	6/1999	(JP)	C30B/29/06
11-180800	7/1999	(JP)	C30B/29/06
11-189495	7/1999	(JP)	C30B/29/06
11-199386	7/1999	(JP)	C30B/29/06
11-199387	7/1999	(JP)	C30B/29/06
WO 97/26393	7/1997	(WO)	C30B/29/06
WO 98/38675	9/1998	(WO)	H01L/21/322
WO 98/45507	10/1998	(WO)	C30B/15/00
WO 98/45508	10/1998	(WO)	C30B/15/00
WO 98/45509	10/1998	(WO) .	
WO 98/45510	10/1998	(WO)	C30B/15/00

OTHER PUBLICATIONS

Jacob, M., et al., "Influence of RTP on Vacancy Concentrations", Mat. Res. Soc. Symp. Proc. vol. 490, pp. 129–134, 1998.

Pagani, M., et al., "Spatial variations in oxygen precipitation in silicon after high temperature rapid thermal annealing", Appl. Phys. Lett., vol. 70, No. 12, pp. 1572–1574, 1997.

Shimura, Fumio, "Semiconductor Silicon Crystal Technology", Academic Press, Inc., San Diego, CA, pp. 361–367, 1989.

Zimmermann, H., et al., "Vacancy Concentration Wafer Mapping in Silicon", J. Crystal Growth, vol. 129 (1993), pp. 582–592, 1993.

Abe, et al., "Defect–Free Surfaces of Bulk Wafers by Combination of RTA and Crystal Growth", (publication information unknown).

Abe, et al., "Innovated Silicon Crystal Growth and Wafering Technologies", Electrochemical Society Proceedings, vol. 97, No. 3, pp. 123–133.

E. Dornberger et al., "The Dependence of Ring Like Distributed Stacking Faults on the Axial Temperature Gradient of Growing Czochralski Silicon Crystals", Electrochemical Society Proceedings, vol. 95–4, (1995), pp. 294–305.

Hara, et al., "Enhancement of Oxygen Precipitation in Quenched Czochralski Silicon Crystals", J. Appl. Phys., vol. 66, No. 8 (1989), pp. 3958–3960.

Jacob, et al., "Determination of Vacancy Concentrations in the Bulk of Silicon Wafers by Platinum Diffusion Experiments", J. Appl. Phys., vol. 82, No. 1 (1997), pp. 182–191.

Kissinger, et al. "A Method for Studying the Grown–In Defect Density Spectra in Czochralski Silicon Wafers", J. Electrochem. Soc., vol. 144, No. 4 (1997), pp. 1447–1456.

A.J.R. de Kock, et al. "The Effect of Doping on the Formation of Swirl Defects in Dislocation–Free Czochralski–Grown Silicon Crystals", Journal of Crystal Growth, vol. 49 (1980), pp. 718–734.

von Ammon et al., "The Dependence of Bulk Defects on the Axial Temperature Gradient of Silicon Crystals During Czochralski Growth", Journal of Crystal Growth, vol. 151 (1995), pp. 273–277.

V. Voronkov et al., "Behaviour and Effects of Intrinsic Point Defects in the Growth of Large Silicon Crystals", Electrochemical Society Proceedings, vol. 97–22 (1997), pp. 3–17.

Voronkov, "The Mechanism of Swirl Defects Formation in Silicon", Journal of Crystal Growth, vol. 59, pp. 625–643.

Winkler, et al., "Improvement of the Gate Oxide Integrity by Modifying Crystal Pulling and Its Impact on Device Failures", J. Electrochem. Soc., vol. 141, No. 5 (1994), pp. 1398–1401.

Dornberger, E., et al., "Simulation of Grown–In Voids in Czochralski Silicon Crystals", Electrochemical Society Proceedings, vol. 97, No. 22, pp. 40–49.

Dornberger, E., et al., "Simulation of Non–Uniform Grown–In Void Distributions in Czochralski Silicon Crystals", Electrochemical Society Proceedings, vol. 98, vol. 1, pp. 490–503.

Dornberger, E., et al., "The Impact of Dwell Time Above 900° C During Crystal Growth on the Gate Oxide Integrity of Silicon Wafers", Electrochemical Society Proceedings, vol. 96, No. 13, pp. 140–151.

Nakamura, Kozo, et al., "Formation Process of Grown–In Defects in Czochralski Grown Silicon Crystals", Journal of Crystal Growth, vol. 180, pp. 61–72, 1997.

Sinno, T., et al., "On the Dynamics of the Oxidation–Induced Stacking–Fault Ring in as–grown Czochralski silicon crystals", Applied Physics Letters, vol. 70, No. 17, pp. 2250–2252, 1997.

Sinno, T., et al., "Point Defect Dynamics and the Oxidation–Induced Stacking–Fault Ring in Czochralski–Grown Silicon Crystals", J. Electrochem. Soc., vol. 145, No. 1, pp. 302–318, 1998.
Tan, T. Y., "Point Defects, Diffusion Processes, and Swirl Defect Formation in Silicon", Appl. Phys. A., vol. 37, pp. 1–17, 1985.
Vanhellemont, J., et al., "Defects in As–Grown Silicon and Their Evolution During Heat Treatments", Materials Science Forum, vol. 258–263, pp. 341–346, 1997.
Herng–Der Chiou, "The Effects of Preheatings on Axial Oxygen Precipitation Uniformity in Czochralski Silicon Crystals", J. Electrochem. Soc., vol. 139, No. 6, Jun., 1992.
Abstract of Japanese Patent No. 8–293589.
Abstract of Japanese Patent No. 9–326396.
Chiou, H.D., et al., "Gettering of Bonded Soi Layers", Proceedings of the International Symposium on Silicon–On– Insulator Technology and Devices pp. 416–423.
Hawkins, G.A., et al., "Effect of Rapid Thermal Processing on Oxygen Precipitation in Silicon", Mat. Res. Soc. Symp. Proc., vol. 104, pp. 197–200, 1988.
Hawkins, G.A., et al., "The Effect of Rapid Thermal Annealing of the Precipitation of Oxygen in Silicon", J. Appl. Phys., vol. 65, No. 9, pp. 3644–3654, 1989.
Mulestagno, L., et al., "Gettering of Copper in Bonded Silicon Wafers", Electrochemical Society Proceedings, vol. 96, No. 3, pp. 176–182.
International Search Report for Application No. PCT/US99/19958, filed Aug. 31, 1999, 11 pages.
Abstract of Japanese Patent No. 59119822.

* cited by examiner

FIG. 1

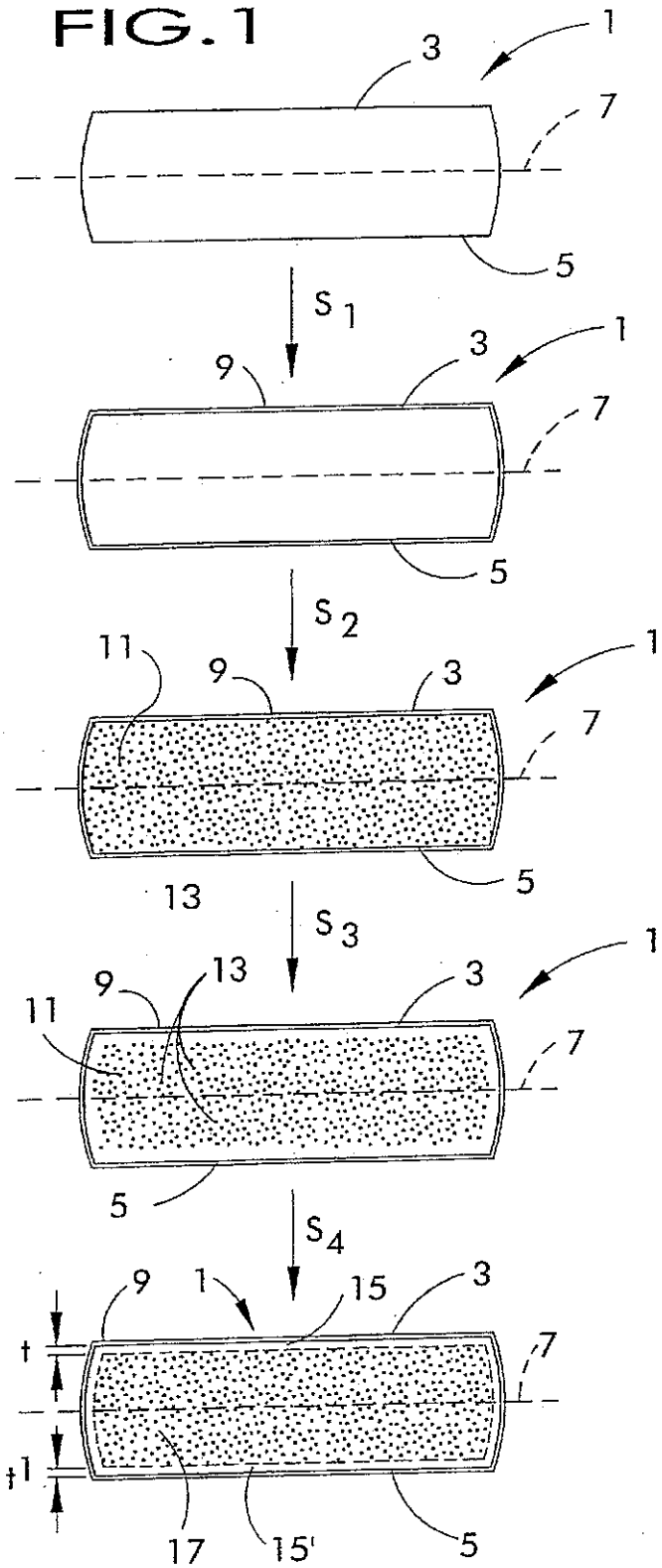


FIG 2

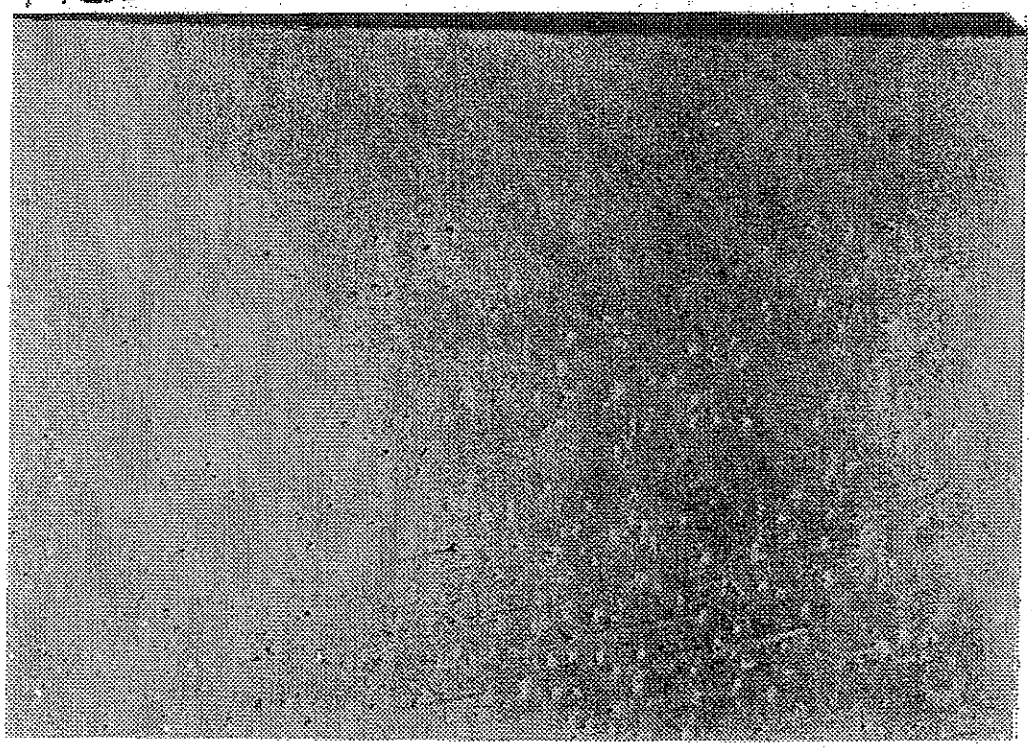


FIG 3

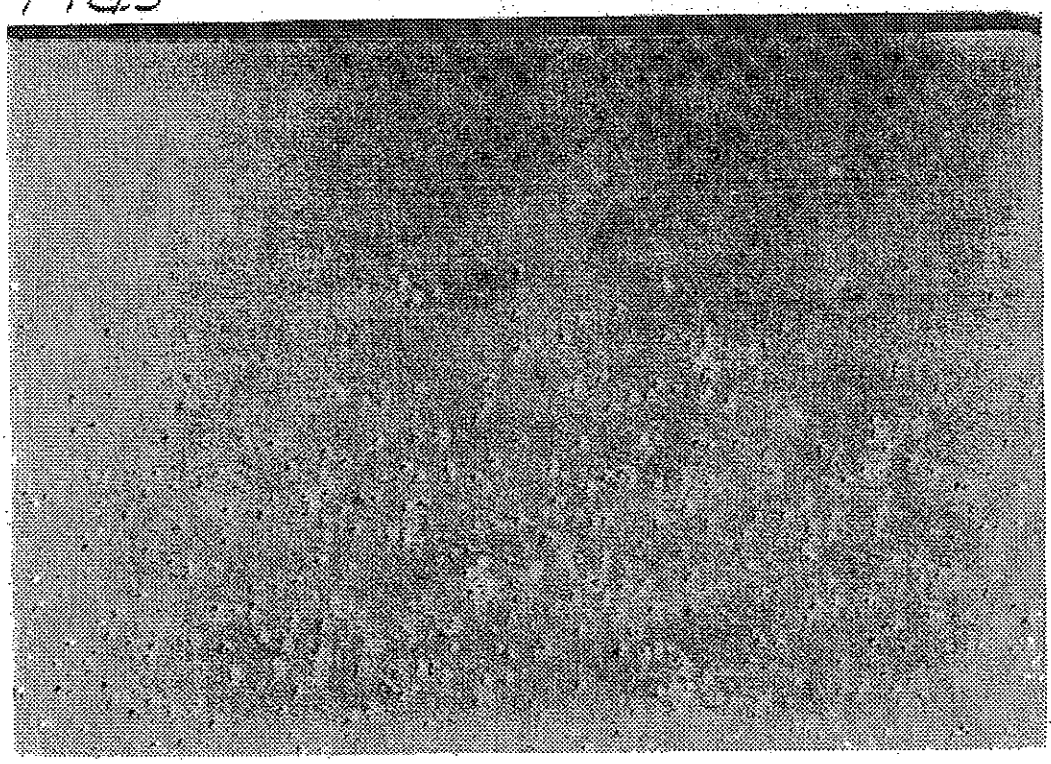


FIG.4

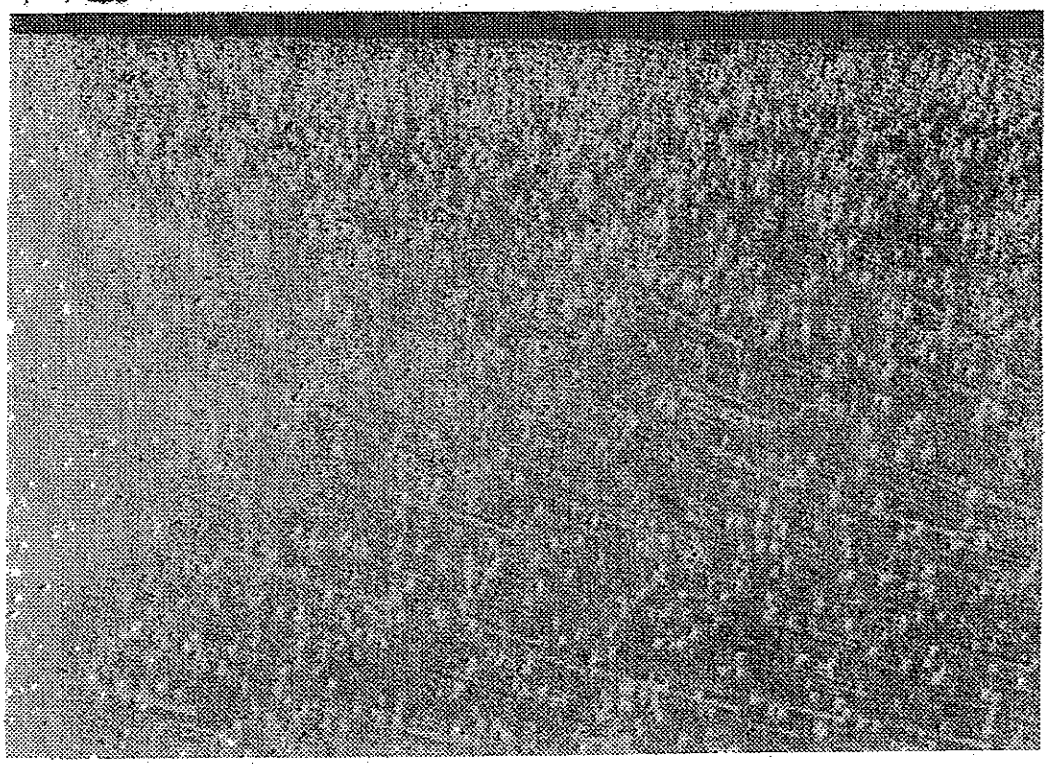


FIG.5

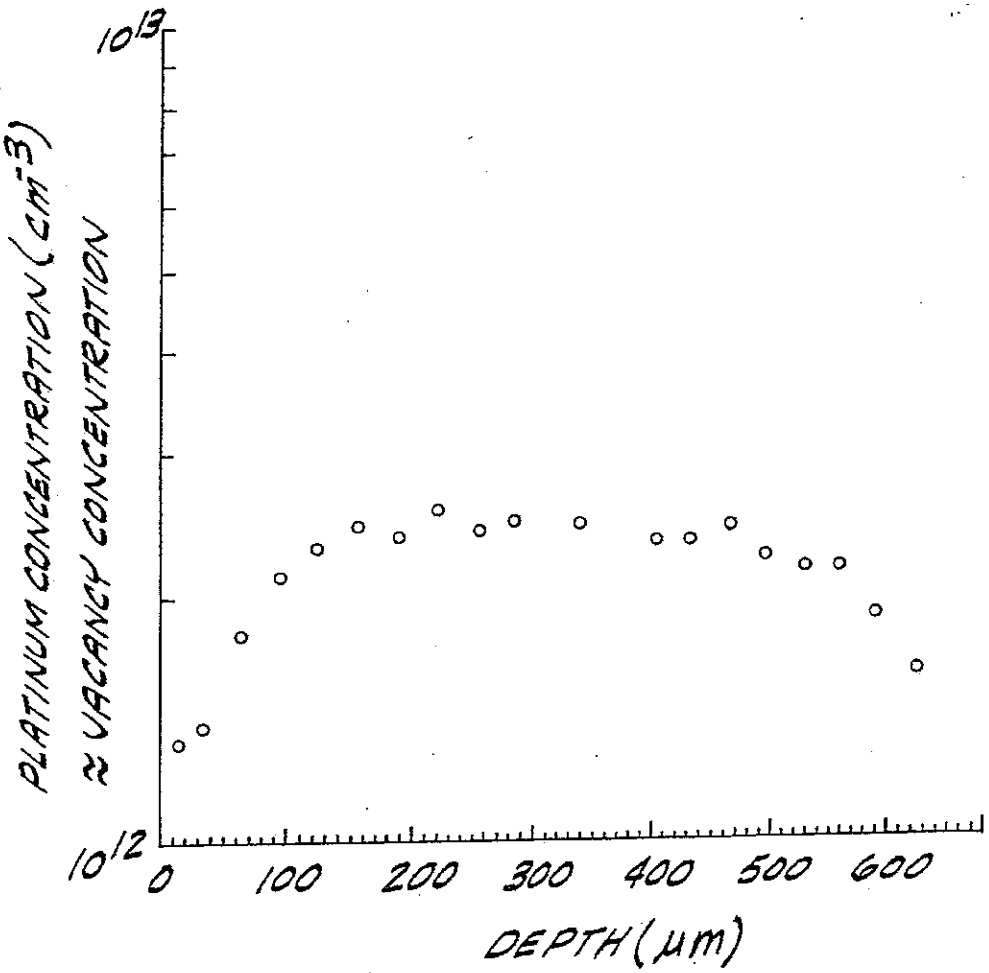

PLATINUM CONCENTRATION (cm-3)
≈ VACANCY CONCENTRATION
10^13
10^12
0
100
200
300
400
500
600
DEPTH (μm)

FIG 6

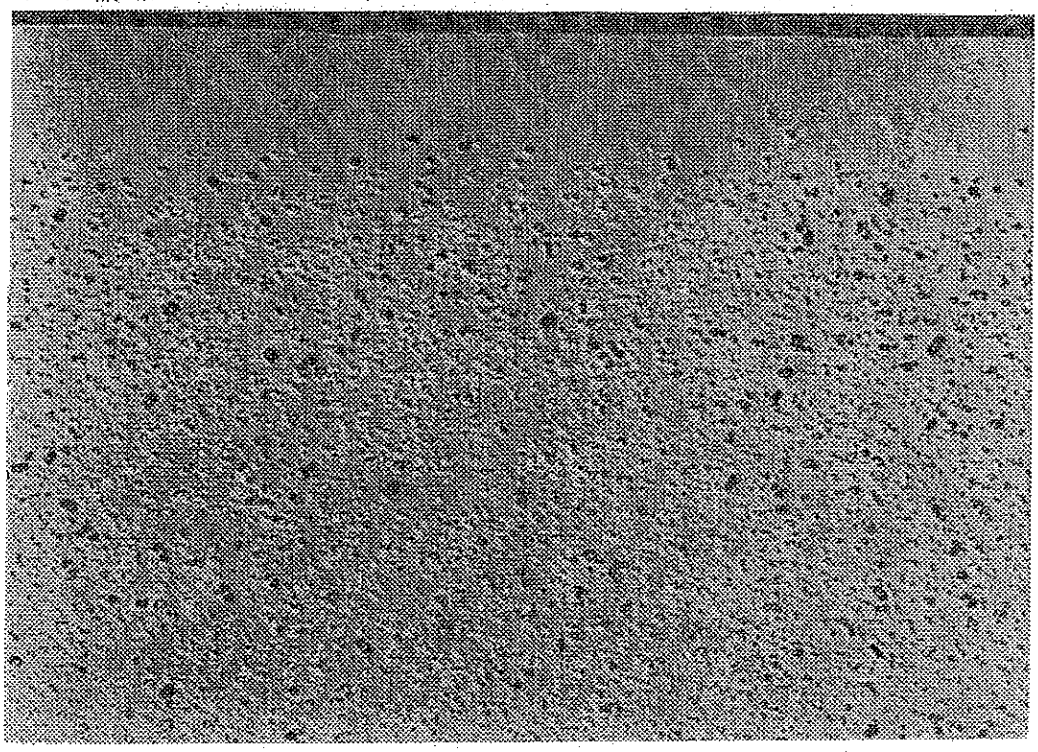


FIG. 7

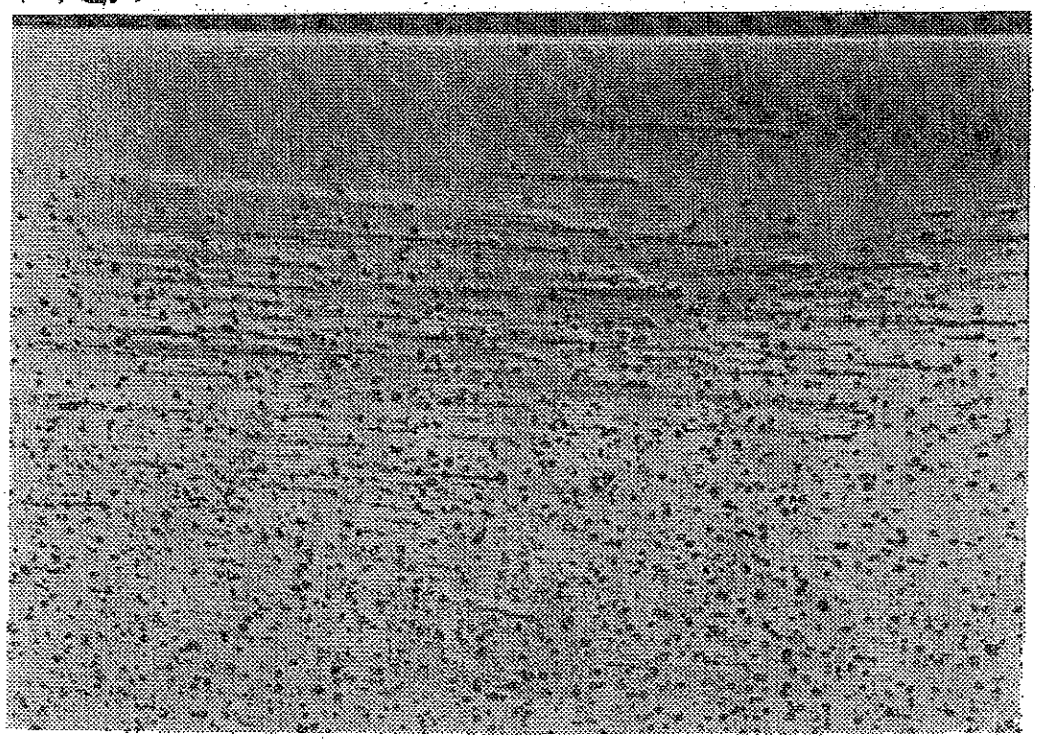


FIG 8

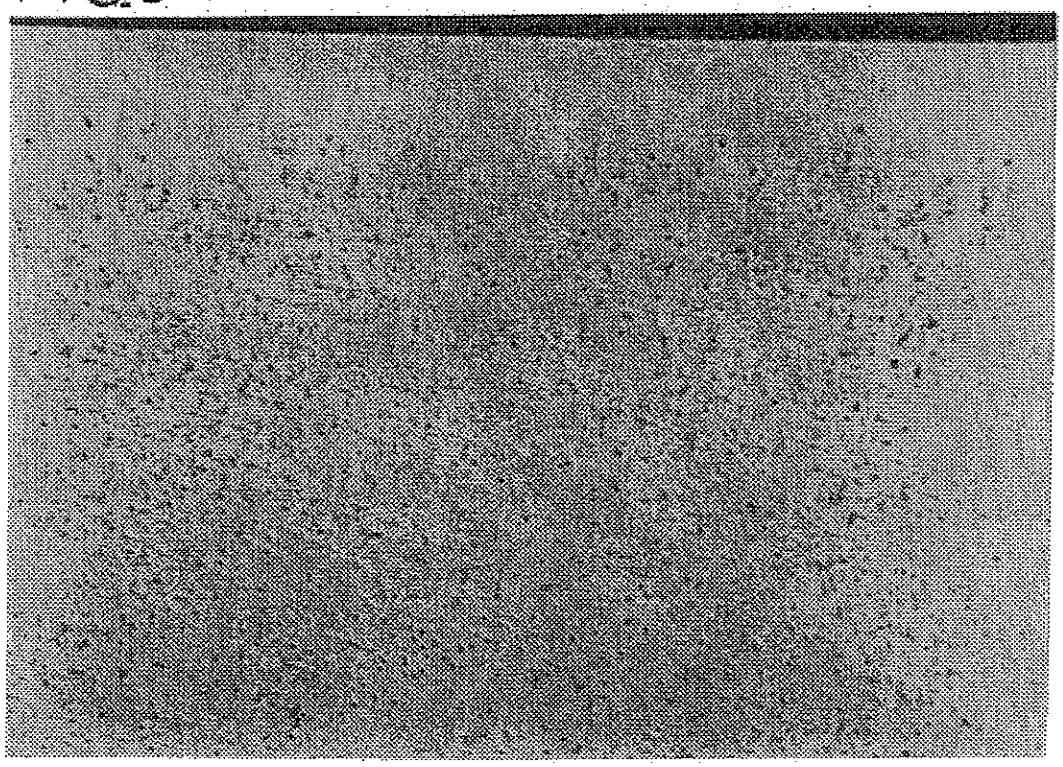


FIG. 9

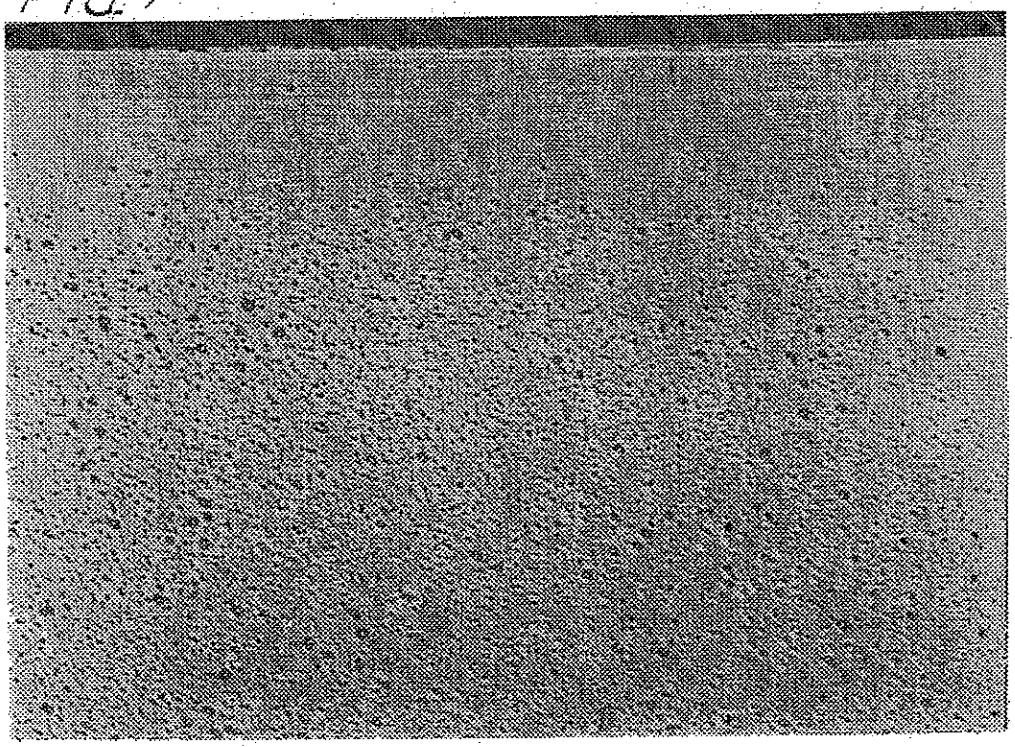


FIG. 10

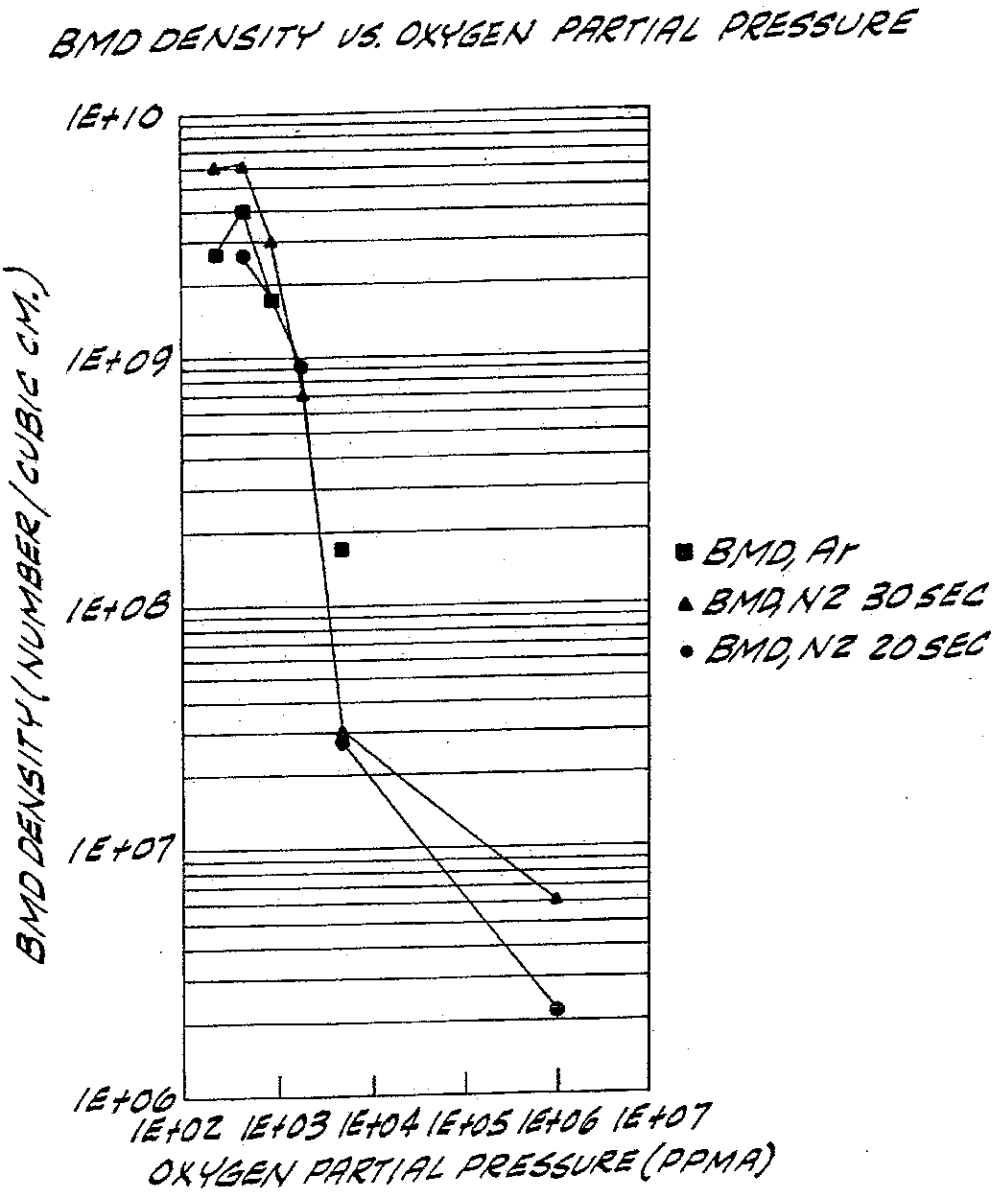

BMD DENSITY VS. OXYGEN PARTIAL PRESSURE
1E+10
1E+09
1E+08
1E+07
1E+06
BMD DENSITY (NUMBER/CUBIC CM.)
1E+02 1E+03 1E+04 1E+05 1E+06 1E+07
OXYGEN PARTIAL PRESSURE (PPMA)
BMD, Ar
BMD, N2 30SEC
BMD, N2 20SEC

FIG.11

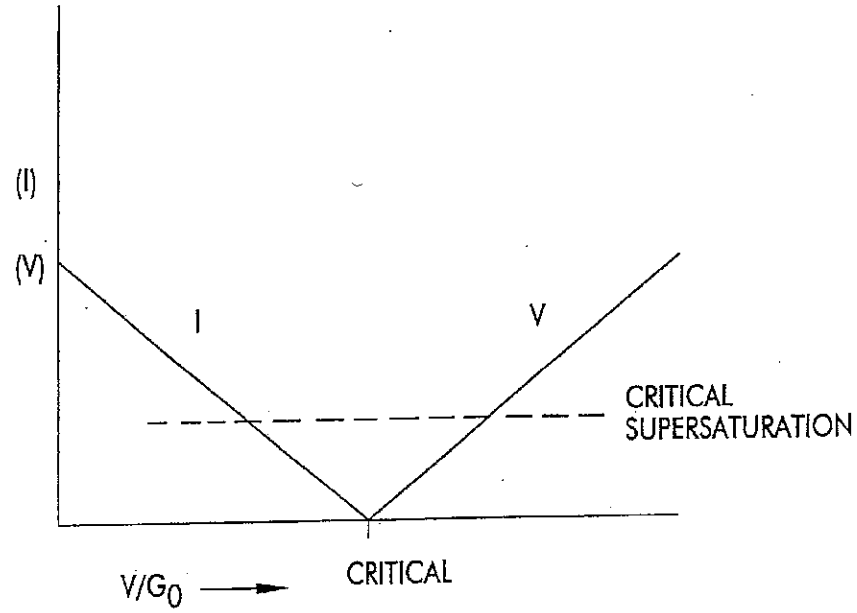

(I)
(V)
I
V
CRITICAL
SUPERSATURATION
V/G0
CRITICAL

FIG.12

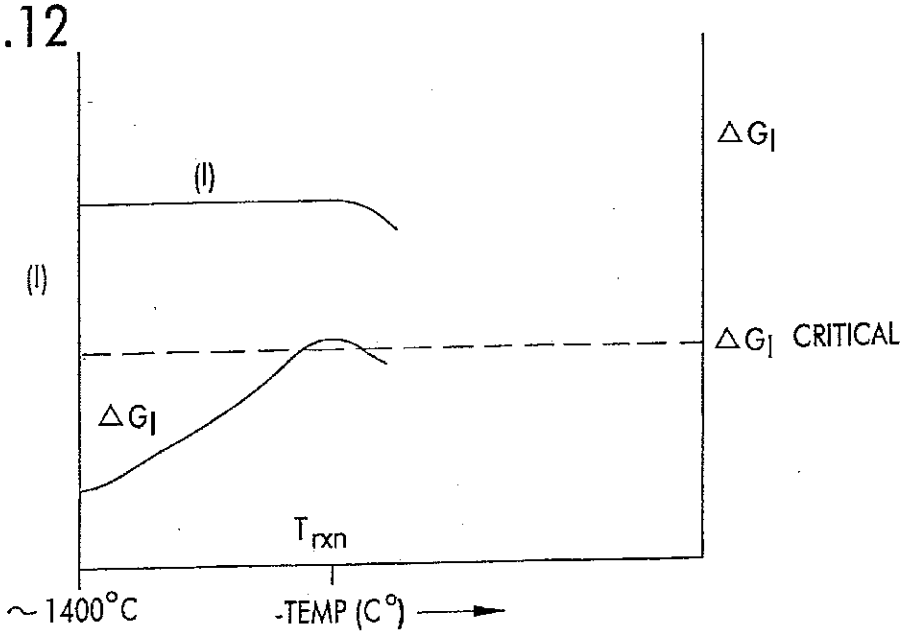

ΔGI
(I)
(I)
ΔGI CRITICAL
ΔGI
Trxn
~1400°C
-TEMP (C°)

FIG.13

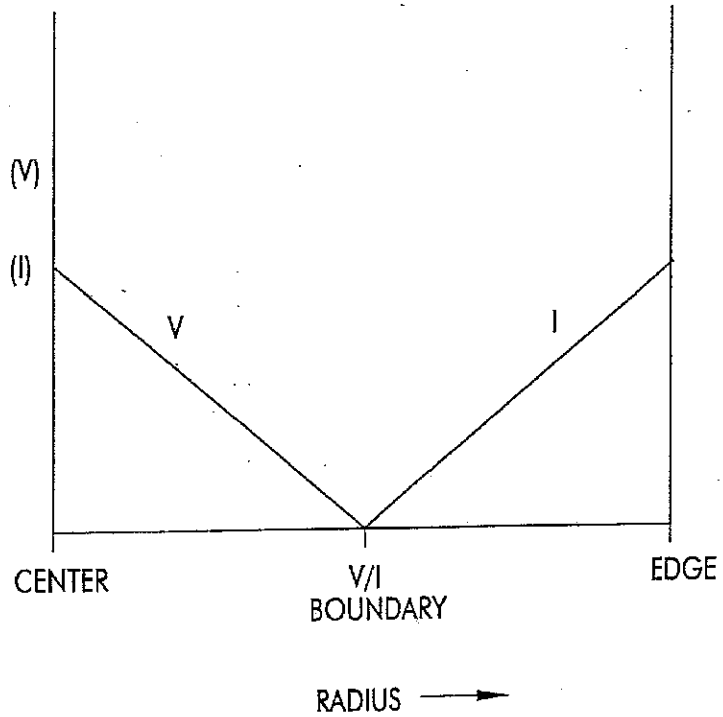

(V)
(I)
V
I
CENTER
V/I BOUNDARY
EDGE
RADIUS

FIG.14

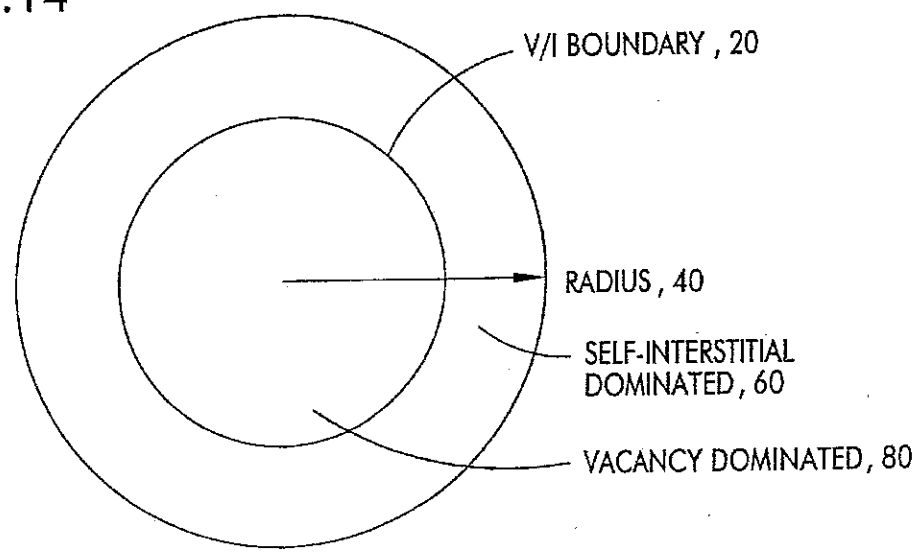

V/I BOUNDARY , 20
RADIUS , 40
SELF-INTERSTITIAL DOMINATED , 60
VACANCY DOMINATED , 80

FIG.15

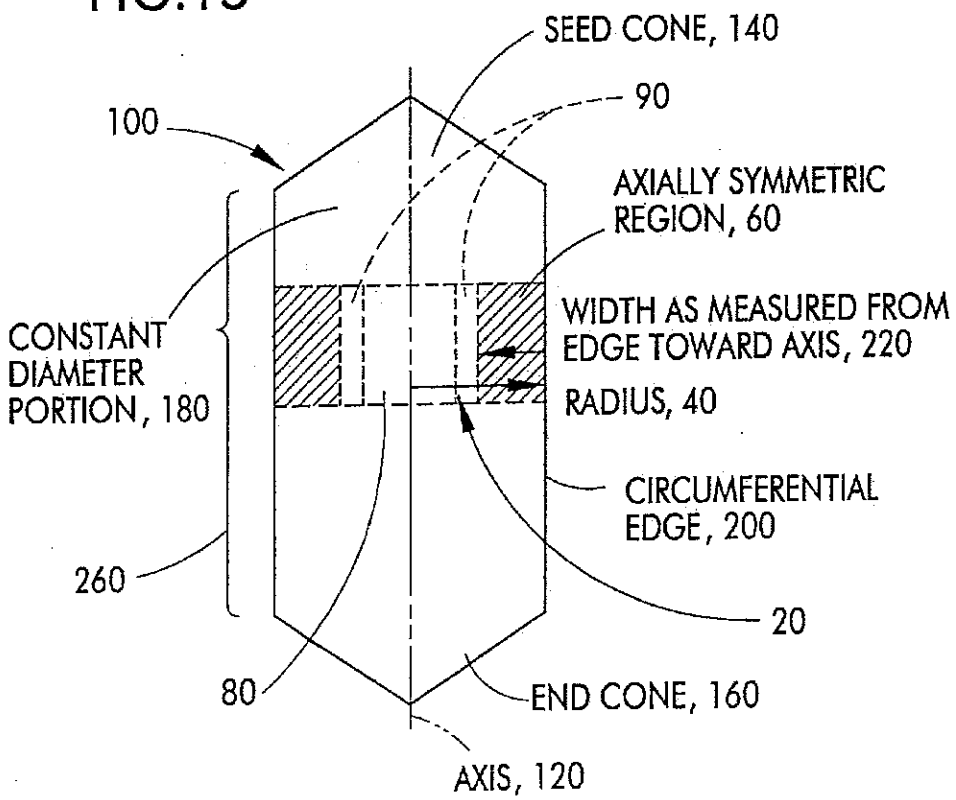
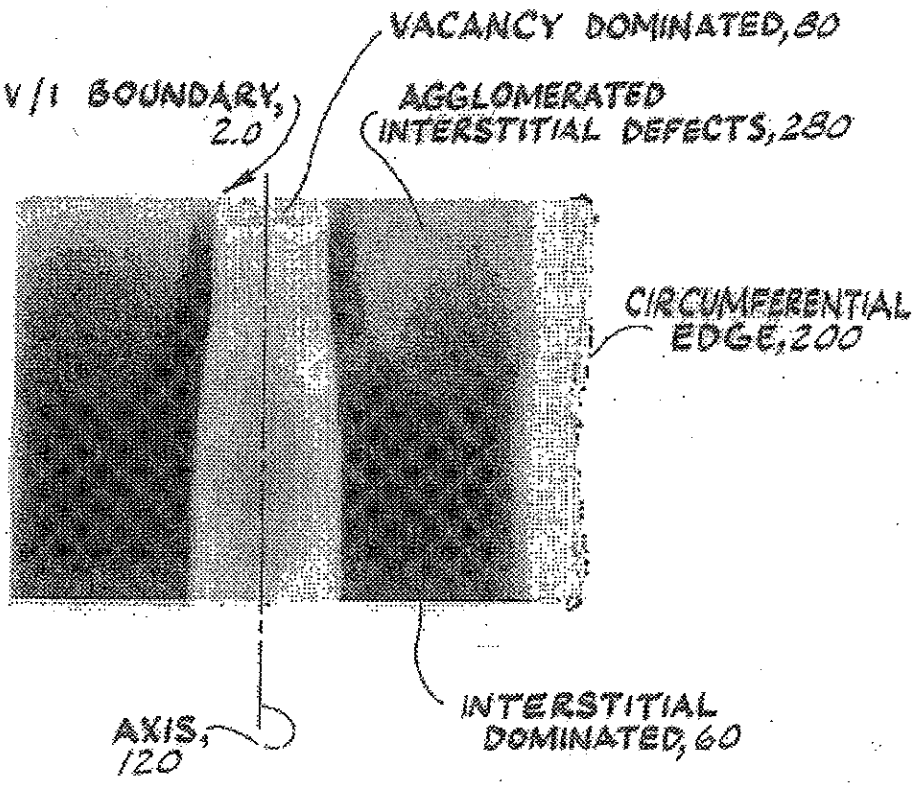

SEED CONE, 140
90
100
AXIALLY SYMMETRIC REGION, 60
WIDTH AS MEASURED FROM EDGE TOWARD AXIS, 220
CONSTANT DIAMETER PORTION, 180
RADIUS, 40
CIRCUMFERENTIAL EDGE, 200
260
20
80
END CONE, 160
AXIS, 120

FIG.16


VACANCY DOMINATED, 60
V/I BOUNDARY, 2.0
AGGLOMERATED INTERSTITIAL DEFECTS, 280
CIRCUMFERENTIAL EDGE, 200
AXIS, 120
INTERSTITIAL DOMINATED, 60